



3.3V 512K × 8 CMOS SRAM

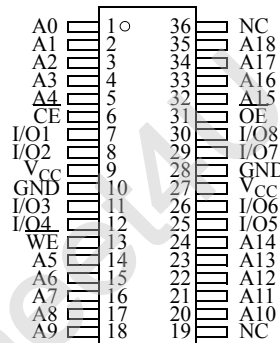
**Features**

- Pin compatible to AS7C34096
- Industrial and commercial temperature
- Organization: 524,288 words × 8 bits
- Center power and ground pins
- High speed
  - 10/12/15/20 ns address access time
  - 4/5/6/7 ns output enable access time
- Low power consumption: ACTIVE
  - 650 mW / max @ 10 ns
- Low power consumption: STANDBY
  - 18 mW / max CMOS

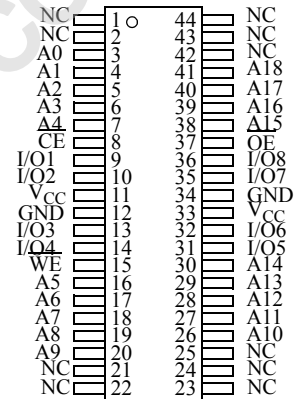
- Equal access and cycle times
- Easy memory expansion with  $\overline{CE}$ ,  $\overline{OE}$  inputs
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400 mil 36-pin SOJ
  - 44-pin TSOP 2
  - 48 pin BGA. 6 X 9mm
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

**Pin arrangements**

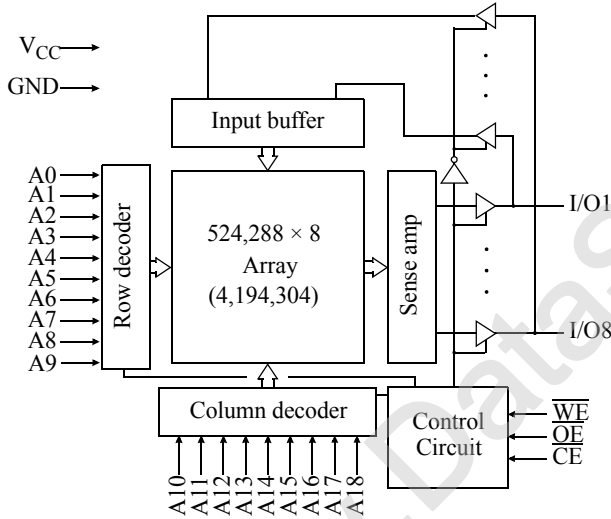
36-pin SOJ (400 mil)



44-pin TSOP 2



**Logic block diagram**



48-pin BGA Package

	1	2	3	4	5	6
A	A <sub>0</sub>	A <sub>1</sub>	NC	A <sub>3</sub>	A <sub>6</sub>	A <sub>8</sub>
B	I/O <sub>5</sub>	A <sub>2</sub>	$\overline{WE}$	A <sub>4</sub>	A <sub>7</sub>	I/O <sub>1</sub>
C	I/O <sub>6</sub>	NC	NC	A <sub>5</sub>	NC	I/O <sub>2</sub>
D	V <sub>SS</sub>	NC	NC	NC	NC	V <sub>CC</sub>
E	V <sub>CC</sub>	NC	NC	NC	NC	V <sub>SS</sub>
F	I/O <sub>7</sub>	NC	A <sub>18</sub>	A <sub>17</sub>	NC	I/O <sub>3</sub>
G	I/O <sub>8</sub>	$\overline{OE}$	$\overline{CE}$	A <sub>16</sub>	A <sub>15</sub>	I/O <sub>4</sub>
H	A <sub>9</sub>	A <sub>10</sub>	A <sub>11</sub>	A <sub>12</sub>	A <sub>13</sub>	A <sub>14</sub>

**Selection guide**

		-10	-12	-15	-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum outputenable access time		4	5	6	7	ns
Maximum operating current	Industrial	180	160	140	110	mA
	Commercial	170	150	130	100	mA
Maximum CMOS standby current		5	5	5	5	mA



## Functional description

The AS7C34096A is a high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 524,288 words  $\times$  8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 10/12/15/20 ns with output enable access times ( $t_{OE}$ ) of 4/5/6/7 ns are ideal for high-performance applications. The chip enable input  $\overline{CE}$  permits easy memory expansion with multiple-bank memory systems.

When  $\overline{CE}$  is high the device enters standby mode. The device is guaranteed not to exceed 18mW power consumption in CMOS standby mode.

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and chip enable ( $\overline{CE}$ ). Data on the input pins I/O1–I/O8 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or  $\overline{CE}$  (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable ( $\overline{OE}$ ) and chip enable ( $\overline{CE}$ ), with write enable ( $\overline{WE}$ ) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 3.3V supply voltage. This device is available as per industry standard 400-mil 36-pin SOJ and 44-pin TSOP 2 packages and also with 48B uBGA package with 6 X 9mm external dimension.

## Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on $V_{CC}$ relative to GND	$V_{t1}$	-0.5	+5.0	V
Voltage on any pin relative to GND	$V_{t2}$	-0.5	$V_{CC} + 0.5$	V
Power dissipation	$P_D$	–	1.0	W
Storage temperature (plastic)	$T_{stg}$	-65	+150	$^{\circ}C$
Temperature with $V_{CC}$ applied	$T_{bias}$	-55	+125	$^{\circ}C$
DC current into output (low)	$I_{OUT}$	–	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
L	H	H	High Z	Output disable ( $I_{CC}$ )
L	H	L	$D_{OUT}$	Read ( $I_{CC}$ )
L	L	X	$D_{IN}$	Write ( $I_{CC}$ )

Key: X = Don't care, L = Low, H = High



### Recommended operating condition

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage	$V_{CC}(10/12/15/20)$	3.0	3.3	3.6	V
Input voltage	$V_{IH}^{**}$	2.0	–	$V_{CC} + 0.5$	V
	$V_{IL}^*$	–0.5	–	0.8	V
Ambient operating temperature	commercial $T_A$	0	–	70	°C
	industrial $T_A$	–40	–	85	°C

\*  $V_{IL}$  min = –1.0V for pulse width less than 5ns.

\*\*  $V_{IH}$  max =  $V_{CC} + 2.0V$  for pulse width less than 5ns.

### DC operating characteristics (over the operating range)<sup>1</sup>

Parameter	Symbol	Test conditions	–10		–12		–15		–20		Unit	
			Min	Max	Min	Max	Min	Max	Min	Max		
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}, V_{IN} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	μA	
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}, \overline{CE} = V_{IH}$ $V_{OUT} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	μA	
Operating power supply current	$I_{CC}$	$V_{CC} = \text{Max}, \overline{CE} < V_{IL}$ $f = f_{\text{Max}}, I_{OUT} = 0\text{mA}$	Industrial	–	180	–	160	–	140	–	110	mA
			Commercial	–	170	–	150	–	130	–	100	mA
Standby power supply current	$I_{SB}$	$V_{CC} = \text{Max}, \overline{CE} = V_{IH}$ $f = f_{\text{Max}}, I_{OUT} = 0\text{mA}$	–	60	–	60	–	60	–	60	mA	
	$I_{SB1}$	$V_{CC} = \text{Max},$ $\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V,$ $f = 0$	–	5	–	5	–	5	–	5	mA	
Output voltage	$V_{OL}$	$I_{OL} = 8\text{mA}, V_{CC} = \text{Min}$	–	0.4	–	0.4	–	0.4	–	0.4	V	
	$V_{OH}$	$I_{OH} = -4\text{mA}, V_{CC} = \text{Min}$	2.4	–	2.4	–	2.4	–	2.4	–	V	

### Capacitance ( $f = 1\text{MHz}, T_a = 25^\circ\text{C}, V_{CC} = \text{NOMINAL}$ )<sup>2</sup>

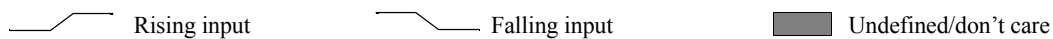
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	A, $\overline{CE}, \overline{WE}, \overline{OE}$	$V_{IN} = 0V$	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{IN} = V_{OUT} = 0V$	7	pF



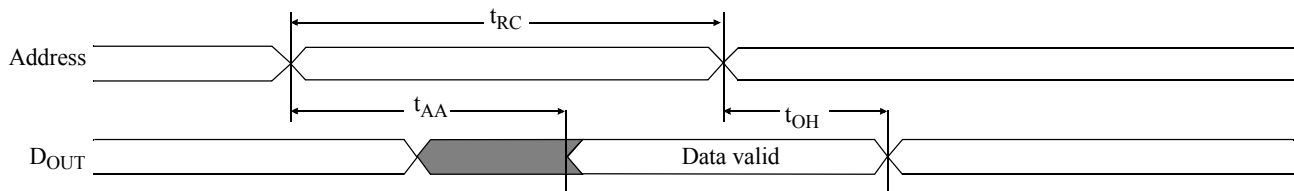
### Read cycle (over the operating range)<sup>3,9</sup>

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	$t_{RC}$	10	–	12	–	15	–	20	–	ns	
Address access time	$t_{AA}$	–	10	–	12	–	15	–	20	ns	3
Chip enable ( $\overline{CE}$ ) access time	$t_{ACE}$	–	10	–	12	–	15	–	20	ns	3
Output enable ( $\overline{OE}$ ) access time	$t_{OE}$	–	4	–	5	–	6	–	7	ns	
Output hold from address change	$t_{OH}$	3	–	3	–	3	–	3	–	ns	5
$\overline{CE}$ Low to output in low Z	$t_{CLZ}$	3	–	3	–	3	–	3	–	ns	4, 5
$\overline{CE}$ High to output in high Z	$t_{CHZ}$	–	5	–	6	–	7	–	9	ns	4, 5
$\overline{OE}$ Low to output in low Z	$t_{OLZ}$	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ High to output in high Z	$t_{OHZ}$	–	5	–	6	–	7	–	9	ns	4, 5
Power up time	$t_{PU}$	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	$t_{PD}$	–	10	–	12	–	15	–	20	ns	4, 5

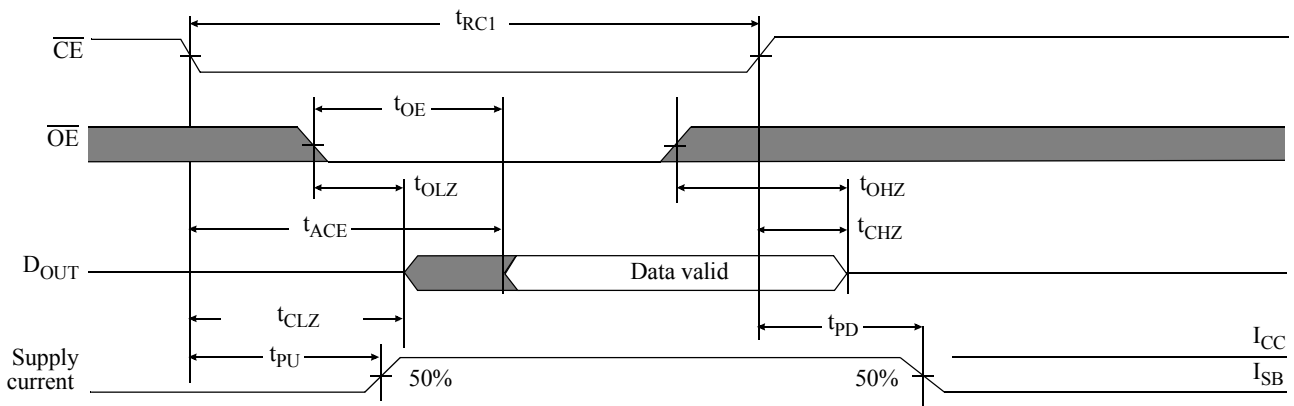
### Key to switching waveforms



### Read waveform 1 (address controlled)<sup>3,6,7,9</sup>



### Read waveform 2 ( $\overline{CE}$ , $\overline{OE}$ controlled)<sup>3,6,8,9</sup>

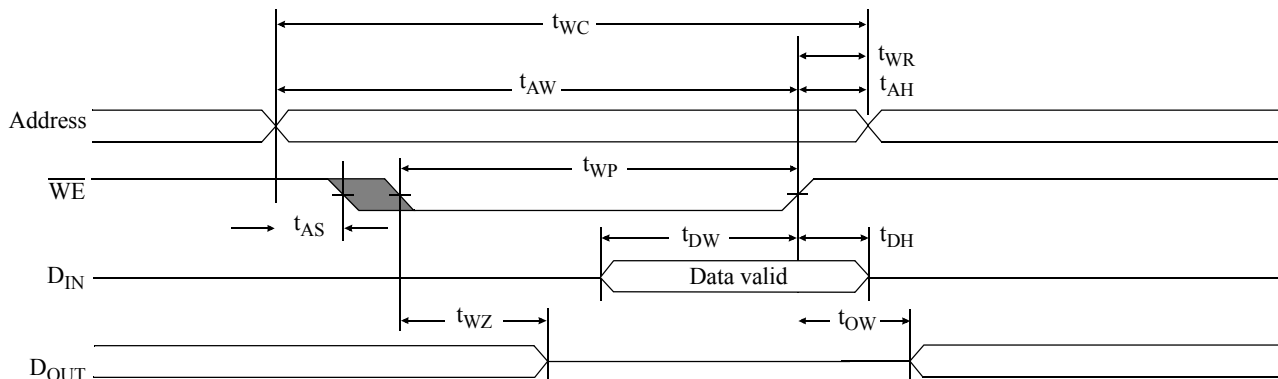




### Write cycle (over the operating range)<sup>11</sup>

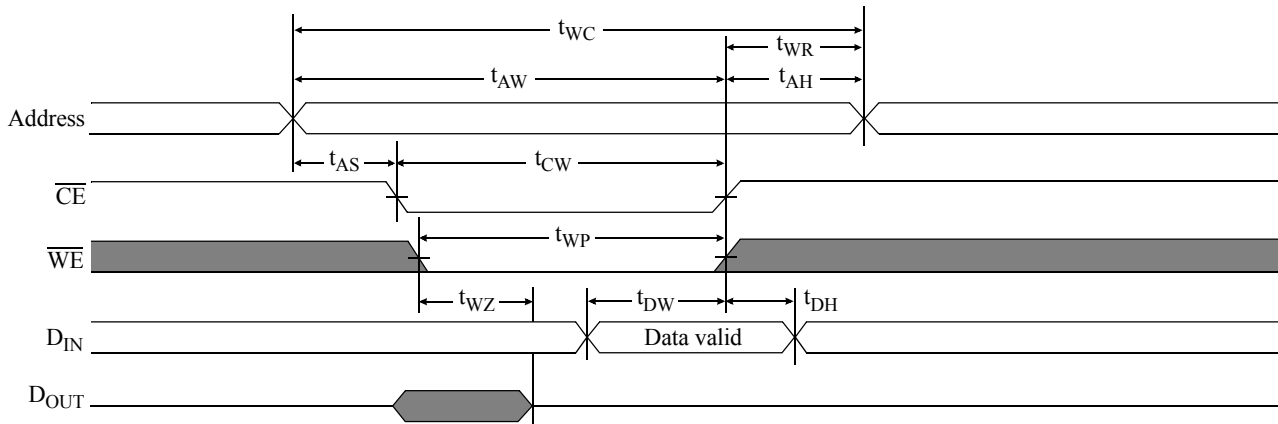
Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	10	–	12	–	15	–	20	–	ns	
Chip enable ( $\overline{CE}$ ) to write end	$t_{CW}$	7	–	8	–	10	–	12	–	ns	
Address setup to write end	$t_{AW}$	7	–	8	–	10	–	12	–	ns	
Address setup time	$t_{AS}$	0	–	0	–	0	–	0	–	ns	
Write pulse width ( $\overline{OE} = \text{high}$ )	$t_{WP1}$	7	–	8	–	10	–	12	–	ns	
Write pulse width ( $\overline{OE} = \text{low}$ )	$t_{WP2}$	10	–	12	–	15	–	20	–	ns	
Address hold from end of write	$t_{AH}$	0	–	0	–	0	–	0	–	ns	
Write recovery time	$t_{WR}$	0	–	0	–	0	–	0	–	ns	
Data valid to write end	$t_{DW}$	5	–	6	–	7	–	9	–	ns	
Data hold time	$t_{DH}$	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in high Z	$t_{WZ}$	0	5	0	6	0	7	0	9	ns	4, 5
Output active from write end	$t_{OW}$	3	–	3	–	3	–	3	–	ns	4, 5

### Write waveform 1 ( $\overline{WE}$ controlled)<sup>10,11</sup>





## Write waveform 2 ( $\overline{\text{CE}}$ controlled)<sup>10,11</sup>



## AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0V. See Figures A and B.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

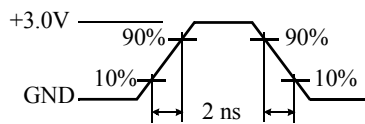


Figure A: Input pulse

Thevenin equivalent:

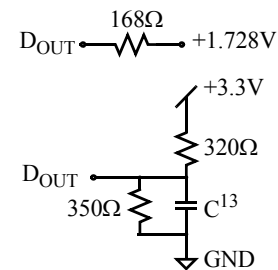


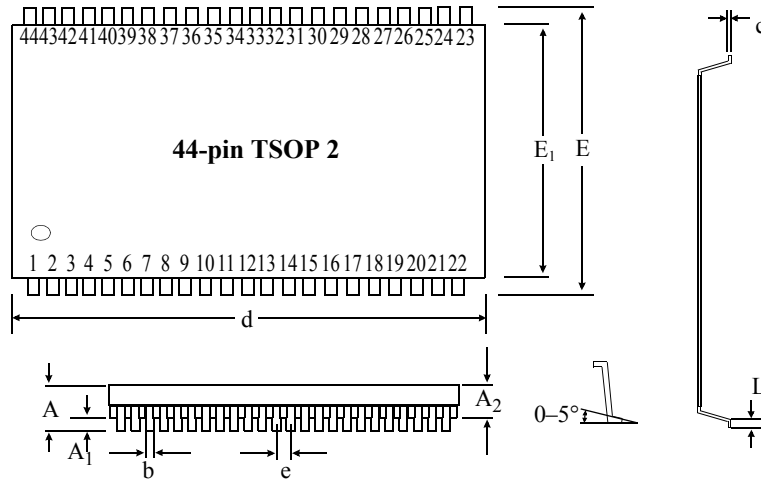
Figure B: 3.3V Output load

## Notes

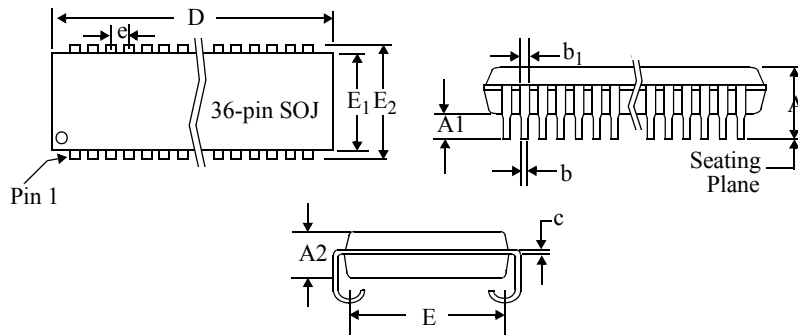
- 1 During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{\text{CE}}$  is required to meet  $I_{SB}$  specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see *AC Test Conditions*.
- 4  $t_{CLZ}$  and  $t_{CHZ}$  are specified with  $C_L = 5\text{pF}$  as in Figure B. Transition is measured  $\pm 500$  mV from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- 6  $\overline{\text{WE}}$  is HIGH for read cycle.
- 7  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  are LOW for read cycle.
- 8 Address valid prior to or coincident with  $\overline{\text{CE}}$  transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 N/A
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 N/A
- 13  $C = 30\text{pF}$ , except on High Z and Low Z parameters, where  $C = 5\text{pF}$ .



Package dimensions



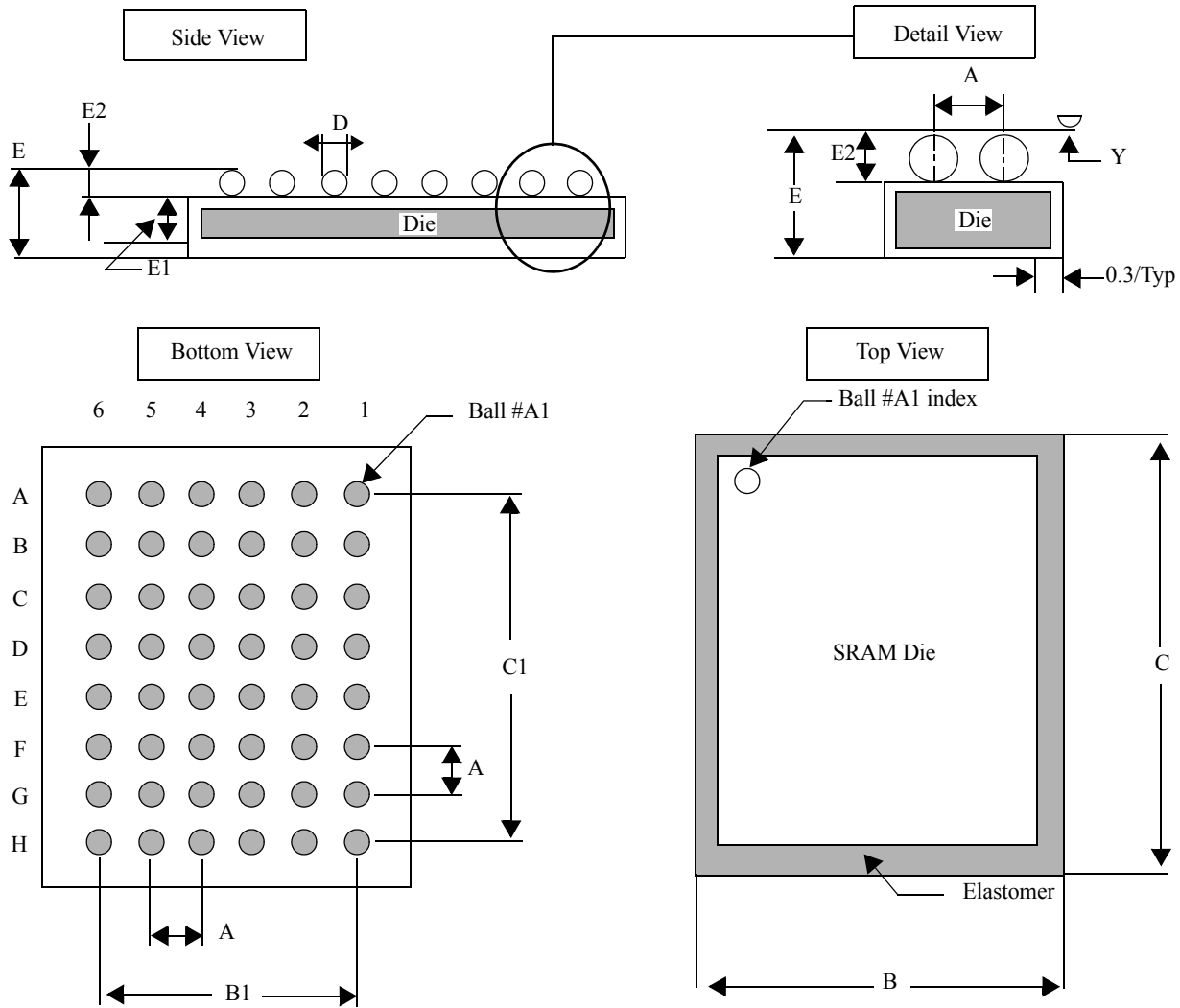
	44-pin TSOP 2	
	Min(mm)	Max(mm)
<b>A</b>		1.2
<b>A<sub>1</sub></b>	0.05	0.15
<b>A<sub>2</sub></b>	0.95	1.05
<b>b</b>	0.30	0.45
<b>c</b>	0.12	0.21
<b>d</b>	18.31	18.52
<b>E<sub>1</sub></b>	10.06	10.26
<b>E</b>	11.68	11.94
<b>e</b>	0.80 (typical)	
<b>L</b>	0.40	0.60



	36-pin SOJ 400	
	Min(mils)	Max(mils)
<b>A</b>	0.128	0.148
<b>A<sub>1</sub></b>	0.025	–
<b>A<sub>2</sub></b>	0.105	0.115
<b>b</b>	0.015	0.020
<b>b<sub>1</sub></b>	0.026	0.032
<b>c</b>	0.007	0.013
<b>D</b>	.920	.930
<b>e</b>	0.045	0.055
<b>E</b>	0.370 BSC	
<b>E<sub>1</sub></b>	0.395	0.405
<b>E<sub>2</sub></b>	0.435	0.445



48-ball FBGA



Notes

1. Bump counts: 48 (8 row × 6 column).
2. Pitch: (x,y) = 0.75 mm × 0.75 mm (typ).
3. Units: millimeters.
4. All tolerance are ±0.050 unless otherwise specified.
5. Typ: typical.
6. Y is coplanarity: 0.10 (max).

48-ball FBGA			
	Minimum	Typical	Maximum
<b>A</b>	–	0.75	–
<b>B</b>	5.90	6.00	6.10
<b>B1</b>	–	3.75	–
<b>C</b>	8.90	9.00	9.10
<b>C1</b>	–	5.25	–
<b>D</b>	0.30	0.35	0.40
<b>E</b>	–	–	1.20
<b>E1</b>	–	0.32	–
<b>E2</b>	0.24	0.27	0.3
<b>Y</b>	–	–	0.10





### Ordering codes

Package	Temperature	10 ns	12 ns	15 ns	20 ns
SOJ	Commercial	AS7C34096A-10JC	AS7C34096A-12JC	AS7C34096A-15JC	AS7C34096A-20JC
	Industrial	AS7C34096A-10JI	AS7C34096A-12JI	AS7C34096A-15JI	AS7C34096A-20JI
TSOP 2	Commercial	AS7C34096A-10TC	AS7C34096A-12TC	AS7C34096A-15TC	AS7C34096A-20TC
	Industrial	AS7C34096A-10TI	AS7C34096A-12TI	AS7C34096A-15TI	AS7C34096A-20TI
BGA	Commercial	AS7C34096A-10BC	AS7C34096A-12BC	AS7C34096A-15BC	AS7C34096A-20BC
	Industrial	AS7C34096A-10BI	AS7C34096A-12BI	AS7C34096A-15BI	AS7C34096A-20BI

**Note:** Add suffix 'N' to the above part number for Lead Free Parts. (Ex: AS7C34096A - 10 TIN)

### Part numbering system

AS7C	X	4096A	-XX	J, T, or B	X	X
SRAM prefix	Voltage: 3 - 3.3V CMOS	Device number	Access time	Packages: J: SOJ 400 mil T: TSOP 2 B: 48-ball FBGA 6x9 mm	Temperature ranges: C: Commercial, 0°C to 70°C I: Industrial, -40°C to 85°C	N=Lead Free Parts



AS7C34096A



Alliance Semiconductor Corporation  
2575, Augustine Drive,  
Santa Clara, CA 95054  
Tel: 408 - 855 - 4900  
Fax: 408 - 855 - 4999  
[www.alsc.com](http://www.alsc.com)

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